REMARKS

This responds to the Office Action mailed February 2, 2004 in the above-identified application. For the following reasons, reconsideration and allowance of the application are respectfully requested. Claims 1-45 are pending in the application. Claims 8-29 and 43-45 have been withdrawn from consideration as directed to a non-elected invention. No claims have been amended. Accordingly, claims 1-7 and 30-42 are under consideration in the present application. Claims 1, 6, 30, 34 and 41 are independent claims.

The Examiner has rejected claims 1-3, 6-7, 30-31, 34-35 and 41-42 under 35 U.S.C. §102(e) as anticipated by Cypher (US 6,289,420). Claims 4-5 and 32-33 are rejected under 35 U.S.C. §103(a) as unpatentable over Cypher in view of Malamy et al. (US 5,675,765). Claims 36-40 are rejected under 35 U.S.C. §103(a) as unpatentable over Cypher in view of Sager et al. (US 6,425,055). The rejections are respectfully traversed.

Cypher discloses a cache memory that includes a plurality of memory chips which are configured to collectively store a plurality of cache lines. Each cache line includes data and an associated cache tag (abstract). Each cache line is stored across the memory chips in a row formed by corresponding entries accessed using the same index address (abstract; Fig. 2 and col. 4, lines 49-65). The plurality of cache lines is grouped into separate subsets based on index addresses, thereby forming several separate classes of cache lines. The cache tags associated with cache lines of different classes are stored in different memory chips (abstract; Fig. 3 and col. 5, lines 8-26). During operation the cache controller may receive multiple snoop requests corresponding to transactions initiated by various processors. The cache controller is configured to concurrently access the cache tags of multiple lines in response to the snoop requests if the lines correspond to differing classes (abstract).

Applicants' claim 1 is directed to a cache memory system comprising a plurality of memory locations for storing data and addresses associated with the data, each of the plurality of memory locations having only a single word line associated therewith, and at least one controller that enables first and second devices to access different ones of the plurality of memory locations concurrently.

The cache memory disclosed by Cypher is very different from the cache memory of the present invention. Cypher permits concurrent access to different classes of cache lines. As

shown in Fig. 3 of Cypher, different classes correspond to different groups of cache lines. By contrast, Applicants' claim 1 enables first and second devices to access concurrently different ones of the plurality of memory locations *in a single word line*. Cypher, by contrast, discloses concurrent access *to different word lines* of a cache memory. For these reasons, claim 1 is clearly and patentably distinguished over Cypher. Accordingly, withdrawal of the rejection of claim 1 under 35 U.S.C. § 102(e) is respectfully requested.

Claims 2-5 depend from claim 1 and are patentable over Cypher for at least the reasons discussed above in connection with claim 1.

Claim 6 is directed to a cache memory system comprising a plurality of memory locations to store data and addresses associated with the data, a plurality of cache outputs for providing data retrieved from the memory locations, and first and second multiplexers having multiplexer inputs coupled to at least some of the memory locations and multiplexer outputs coupled to the plurality of cache outputs so as to enable the first and second multiplexers to select data from different ones of the plurality of memory locations to be provided concurrently on respective ones of the plurality of cache outputs.

Cypher does not disclose or suggest a cache memory system including *first and second multiplexers having multiplexer inputs coupled to memory locations and multiplexer outputs coupled to cache outputs* so as to enable first and second multiplexers to select data from different ones of the memory locations to be provided concurrently on respective ones of the plurality of cache outputs, as required by claim 6. Cypher discloses no multiplexers of any type. For these reasons, claim 6 is clearly and patentably distinguished over Cypher. Accordingly, withdrawal of the rejection of claim 6 under 35 U.S.C. § 102(e) is respectfully requested.

Claim 7 depends from claim 6 and is patentable over Cypher for at least the reasons discussed above in connection with claim 6.

Claim 30 is directed to a method of operating an associative cache having a plurality of memory locations for storing data, each of the plurality of memory locations having only a single word line associated therewith. The method comprises concurrently accessing with first and second devices different ones of the plurality of memory locations of the associative cache.

Claim 30 is clearly patentable over Cypher for at least the reasons discussed above in connection with claim 1. In particular, Cypher does not disclose or suggest concurrently

accessing with first and second devices different memory locations each having only a single word line associated therewith. Cypher discloses concurrent access to different word lines of a cache memory. For these reasons, claim 30 is clearly and patentably distinguished over Cypher. Accordingly, withdrawal of the rejection of claim 30 under 35 U.S.C. §102(e) is respectfully requested.

Claims 31-33 depend from claim 30 and are patentable over Cypher for at least the reasons discussed above in connection with claims 1 and 30.

Claim 34 is directed to a method of operating an associative cache having a plurality of memory locations for storing data, and a plurality of outputs for providing data retrieved from the memory locations to respective devices, each of the plurality of memory locations having only a single word line associated therewith. The method includes concurrently providing data from different ones of the plurality of memory locations to the respective devices via the plurality of outputs.

As discussed above in connection with claims 1 and 6, Cypher contains no disclosure or suggestion of concurrently providing data from different memory locations to respective devices, wherein the memory locations have only a single word line associated therewith. Cypher discloses concurrent access to different word lines of a cache memory. For these reasons, claim 34 is clearly and patentably distinguished over Cypher. Accordingly, withdrawal of the rejection of claim 34 under 35 U.S.C. §102(e) is respectfully requested.

Claims 35-40 depend from claim 34 and are patentable over Cypher for at least the reasons discussed above in connection with claims 1, 6 and 34.

Claim 41 is directed to a cache memory system comprising a plurality of memory locations for storing data and addresses associated with the data, each of the plurality of memory locations having only a single word line associated therewith, and means for enabling first and second devices to access different ones of the plurality of memory locations concurrently.

Claim 41 is clearly patentable over Cypher for at least the reasons discussed above in connection with claim 1. Accordingly, withdrawal of the rejection of claim 41 under 35 U.S.C. §102(e) is respectfully requested.

Claim 42 depends from claim 41 and is patentable over Cypher for at least the reasons discussed above in connection with claims 1 and 41.

CONCLUSION

In view of the foregoing remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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